An Easy-Driving Incremental Zoom ADC With Skipped Sampling Scheme and NS-SAR Quantizer

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***Abstract*—This article presents an incremental zoom analog-to-digital converter (ADC) for Internet-of-Things (IoT) applications. Unlike prior zoom ADC designs, a floating inverter amplifier (FIA)-assisted residue extraction scheme is proposed to maintain the residue voltage during loop filtering. It allows the ADC to skip repeated sampling operations between consecutive fine conversions, thus largely reducing the sampling time and driving cost. To speed up the conversion, a high-efficiency second-order single buffer embedded noise-shaping (NS) successive approximation register (SAR) is proposed as the fine quantizer, allowing a low conversion cycle of 32. Together with the amplifier-reused kT/C noise cancellation technique, the prototype ADC fabricated in a 28-nm CMOS realizes a 92.5-dB SNDR at 300 kS/s with a small input capacitor of 0.8 pF. With fully dynamic operation, the power consumption is only 160 μW, leading to a superior Schreier figure of merit (FoM) of 182.2 dB.**

***Index Terms*—Analog-to-digital converter (ADC), dynamic amplifier, incremental zoom ADC, noise shaping (NS), successive approximation register (SAR).**

I. Introduction

ADVANCED Internet-of-Things (IoT) applications demand analog-to-digital converters (ADCs) with high energy efficiency and high resolution for long-term, high-quality sensor readout. These ADCs should also feature medium conversion speed (hundreds of kilohertz) and easy system integration for wider application spans. Among the general ADC architectures, the successive approximation register (SAR) ADC has demonstrated superior power efficiency by leveraging highly digital building blocks. However, SAR ADC's power efficiency degrades when targeting high resolution due to the stringent noise requirements of sampling and comparison. ΔΣ modulators (ΔΣMs) suit high-resolution applications thanks to the NS capability. Recently, incremental ΔΣMs have drawn rising attention by favoring system integration and simple digital filtering [1], [2], [3], [4], [5]. The incremental ΔΣMs' resolution depends heavily on the loop filter, which necessitates either a high-order loop filter [1], [2], [3] or large conversion cycles [4], [5], both limiting the energy efficiency.

By performing a low-cost coarse conversion before the performance-critical fine conversions, the zoom architecture relaxes the resolution requirement and power consumption of the fine quantizer. It provides a promising solution for realizing both high resolution and high energy efficiency. In conventional designs, a single-bit ΔΣM with operational transconductance amplifier (OTA)-based integrator is usually adopted as the fine quantizer in zoom ADCs, thus requiring large conversion cycles for targeted resolution [6], [7], [8]. Moreover, due to the charge transfer in the OTA-based integrator, a dedicated input sampling should be performed after each integration to reconstruct the residue voltage. The repeated input sampling operations largely increase the required conversion cycles and incur additional input driving costs. Extra coarse conversions are required to prevent the ΔΣM from overloading, further restricting the conversion rates. As a result, conventional zoom ADCs can only convert quasi-static signals (e.g., 12.5 Hz in [6]). Dynamic zoom ADCs extend the input bandwidth to tens of kilohertz by performing coarse and fine conversions concurrently [9], [10], [11]. Nevertheless, with higher conversion speed, the time and driving cost of repeated sampling operations become more pronounced. Continuous-time (CT) zoom ADCs feature easy driving and intrinsic anti-aliasing characteristics [12], [13], [14]. Yet, limited by the static power-consuming integrators, the energy efficiency of CT zoom ADCs is generally limited. In summary, achieving both medium conversion speed and low driving cost while maintaining high resolution and high energy efficiency is challenging for prior zoom ADC architectures.

Recently, by employing a multi-level SAR quantizer, the emerged NS-SAR ADC demonstrates the high capability of supporting a bandwidth of hundreds of kilohertz with high energy efficiency [15], [16], [17], [18], [19]. However, without the initial coarse quantization as in zoom architecture, high loop filter orders are usually required for high-resolution applications, raising significant hardware cost and design complexity.

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In this article, we present an incremental zoom ADC using NS-SAR as its fine quantizer, integrating the advantages of both zoom ADC and NS-SAR ADC. Compared to conventional zoom ADCs, the conversion cycles are significantly reduced by leveraging a multi-bit NS-SAR quantizer, thus improving the conversion speed. Unlike traditional NS-SAR ADCs, the initial coarse quantization in the zoom architecture eliminates the necessity for a high-order loop filter, reducing the hardware cost and design complexity. Furthermore, only one dynamic buffer is required to realize the proposed second-order loop filter, ensuring its high energy efficiency. To ease the driving requirement, a floating inverter amplifier (FIA)-assisted residue extraction scheme is proposed to perform the loop filtering without destructing the residue voltage. This approach allows multiple successive fine conversions without resampling, thereby skipping 75% sampling operations. In addition, by reusing the FIA, kT/C noise cancellation is performed, reducing the sampling capacitance by 10 times. A digital slope (DS) ADC with second-order digital prediction is proposed as the coarse quantizer that efficiently tracks the input with minimum digital-to-analog converter (DAC) switching activity. Prototyped in 28-nm CMOS, the proposed incremental zoom ADC realizes 92.5-dB signal-to-noise-and-distortion ratio (SNDR) with a conversion rate of 300 kS/s while consuming only 160 μW, leading to 182.2-dB Schreier figures of merit (FoMs).

This article extends the work presented in [20] by thoroughly analyzing the proposed skipped sampling scheme, the NS-SAR fine quantizer, and the DS coarse quantizer. It includes comprehensive simulation results to validate the robustness of the proposed techniques. Furthermore, it offers new measurement results including the Nyquist input results and SNDR variations across temperatures and voltages.

This article is organized as follows. Section II introduces the architecture-level design of the proposed incremental zoom ADC with the skipped sampling scheme, analyzes the noise performance, and describes the proposed three-mode reconfigurable FIA. Section III reviews prior loop filter designs in NS-SAR and introduces the proposed NS-SAR quantizer with the single buffer embedded loop filter. Section IV presents the detailed circuit implementation including the DS coarse quantizer with second-order digital prediction. Section V shows the measurement results. The conclusion is drawn in Section VI.

II. Proposed Incremental Zoom ADC

The simplified block and timing diagrams of the proposed incremental zoom ADC are shown in Fig. 1. It consists of a DS coarse quantizer and an NS-SAR backend. The incremental ADC first samples the input V_{IN}, followed by the DS ADC for coarse conversion. The DS output is then used to determine the NS-SAR reference range. The DS and NS-SAR DACs are merged for better matching. Thanks to the multi-bit fine conversion performed by NS-SAR, the proposed zoom ADC can achieve high resolution with low conversion cycles. To improve the energy efficiency of the NS-SAR fine quantizer, a single buffer embedded loop filter is proposed and will be introduced in Section III.

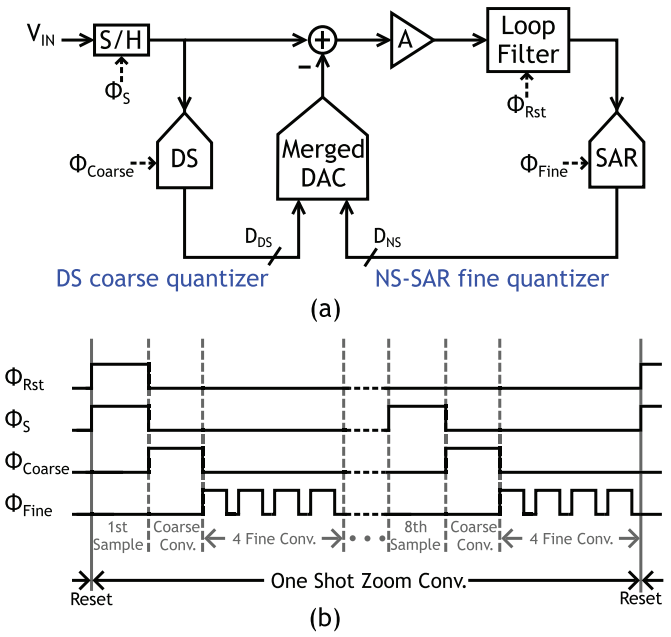

Fig. 1. (a) Simplified diagram of the proposed incremental zoom ADC. (b) ADC timing diagram for one-shot incremental zoom conversion.

An amplifier is employed before the loop filter to attenuate backend noise and prevent destructive charge transfer from the merged DACs. Therefore, multiple consecutive fine conversions can be performed without repeated sampling operations as in conventional zoom ADCs, leading to low driving costs. In one-shot incremental zoom conversion, 32 fine conversions are performed for the targeted accuracy while requiring only eight sampling operations. This skipped sampling scheme will be detailed in Section II-A. Furthermore, the amplifier is reused to perform kT/C noise cancellation, ensuring low kT/C noise with a small sampling capacitor. A three-mode reconfigurable FIA is designed for high energy efficiency. The ADC operations and noise analysis will be discussed in Section II-B, and the proposed three-mode reconfigurable FIA will be shown in Section II-C.

A. Skipped Sampling Scheme

The operation comparison between conventional and proposed zoom ADCs is shown in Fig. 2. At the start of one-shot incremental zoom conversion, the input signal V_{IN} is bottom-plate sampled on C_{DAC}. After the coarse conversion, the coarse conversion result D_{DS}/D_{SAR} is applied to the bottom-plate switches of C_{DAC}, obtaining the residue voltage V_{RES} on the top plate of C_{DAC}. The residue voltage is used for the subsequent fine conversion, after which the residue voltage is updated. During loop filtering, in conventional zoom ADC, residue integration is typically performed by an OTA-based integrator. The OTA forces its input voltage to the virtual ground by the closed-loop charge transfer. The residue voltage stored on C_{DAC} is equivalently discharged during this charge transfer process. As a result, a repeated sampling operation is required in each conversion cycle to reconstruct the residue voltage, which incurs extra driving costs and degrades the conversion speed. With the input signal varying, the fine

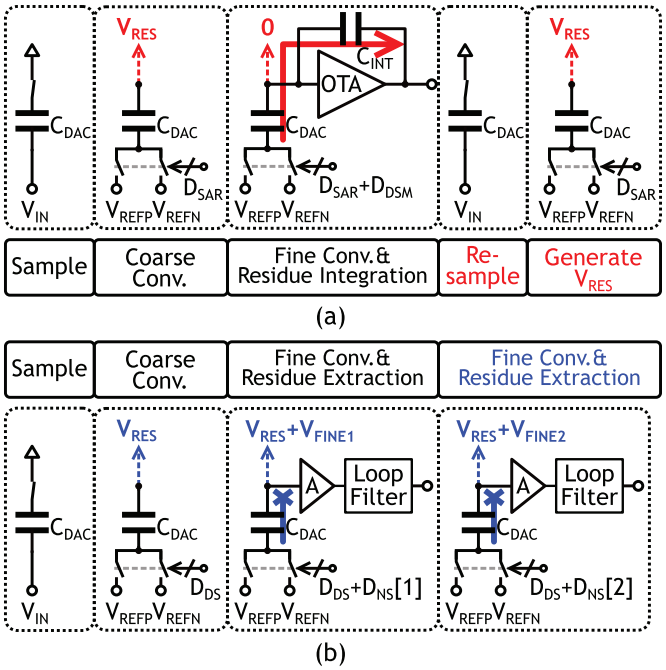

Fig. 2. Comparison between (a) conventional OTA-based ADC and (b) proposed zoom ADC with skipped sampling scheme.

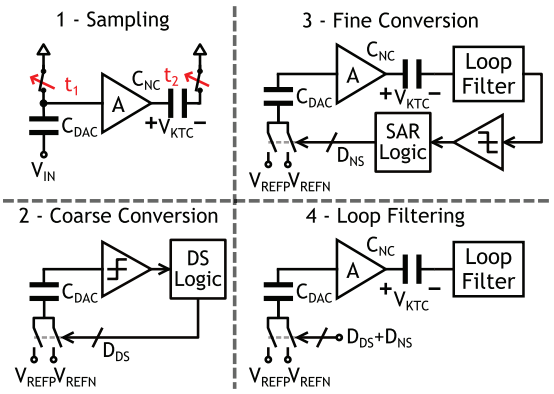

Fig. 3. Circuit configurations in different operational phases of the proposed zoom ADC.

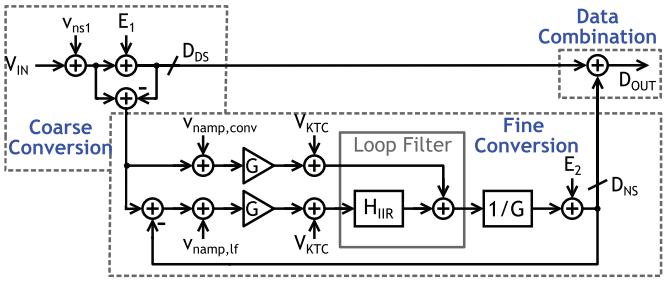

Fig. 4. Signal diagram of the proposed incremental zoom ADC with sampling and amplifier noise.

quantizer converts a different input in each conversion cycle, thus necessitating the careful design of the over-ranging factor between coarse and fine conversions [6], [7], [9], [10].

To address this challenge, an open-loop amplifier is embedded before the loop filter in the proposed zoom ADC. With the amplifier, residue extraction can be performed for loop filtering without destructive charge transferring, thereby maintaining the residue voltage on C_{DAC}. The amplifier also attenuates the input-referred noise of the backend loop filter, allowing for a low-power loop filter design. After the amplifier-assisted loop filtering, by simply resetting the fine DAC output, the coarse residue voltage V_{RES} can be easily regenerated, and thus, the following fine conversion can be performed directly on C_{DAC}, eliminating the dedicated sampling operation as in conventional zoom ADC. Furthermore, throughout multiple fine conversions, the sampled input signal is frozen on C_{DAC}, allowing the fine quantizer to convert the same input multiple times, thereby reducing the quantization error and mitigating the risk of fine quantizer saturation due to varying input signals. It also allows the coarse conversion to be performed only once after the input sampling. Thanks to the proposed skipped sampling scheme, only eight samples and coarse quantizations are required for 32 fine conversion cycles, largely reducing the driving cost and timing overhead.

B. Detailed Operations and Noise Analysis

The ADC operation includes four phases, as illustrated in Fig. 3. During the sampling phase, kT/C noise cancellation is performed by reusing the embedded amplifier. The kT/C noise v_{ns1} is first sampled on C_{DAC} in t_1 moment. It will be amplified and stored on C_{NC} in t_2 moment, together with the input signal change and back-end kT/C noise v_{ns2}. The analysis in [21] reveals the voltage stored on C_{NC} as

$$V_{\mathrm{KTC}} = G \cdot (V_{\mathrm{IN}}(t_2) - V_{\mathrm{IN}}(t_1) - v_{\mathrm{ns1}} + v_{\mathrm{namp,ktc}}) + v_{\mathrm{ns2}} \quad (1)$$

where G is the amplifier's gain and $v_{\mathrm{namp,ktc}}$ is the input-referred noise of the amplifier during kT/C noise amplification. Since V_{KTC} contains the input signal changes between t_1 and t_2, the amplifier's output swing is dependent on the input amplitude and frequency. To ensure a high-linearity amplification with full-scale Nyquist-frequency input, the amplifier's gain G is designed as 10 in this work, which also sufficiently attenuates the backend noise. After sampling, in contrast to [21] and [22], the coarse conversion is directly performed on C_{DAC} instead of after C_{NC}, and thus, the amplifier can be disabled to save power. The coarse conversion result D_{DS} can be calculated as

$$D_{\mathrm{DS}} = V_{\mathrm{IN}}(t_1) + v_{\mathrm{ns1}} + E_1 \quad (2)$$

where E_1 is the coarse residue voltage. Thereafter, during critical fine conversions, the residue voltage is amplified and converted by the NS-SAR quantizer together with V_{KTC} stored on the C_{NC}. A four-LSB inter-stage redundancy is allocated by setting the NS-SAR reference range to five coarse LSBs, which covers the V_{KTC}-induced error and also compensates for the offset of a coarse-stage comparator. Once the NS-SAR quantization finishes, the residue voltage is amplified for the loop integration. If the amplifier's gain remains unchanged during the fine conversion and loop filtering, the kT/C noise v_{ns1} can be naturally canceled, similar to the amplifier's offset and flicker noise [21].

The signal diagram of the proposed incremental zoom ADC with the amplifier's noise and sampling kT/C noise can be depicted in Fig. 4. The loop filter's transfer function, H_{IIR}, is $(2z^{-1} - z^{-2})/(1 - z^{-1})^2$. $v_{\mathrm{namp,conv}}$ and $v_{\mathrm{namp,lf}}$ are the input-referred noise of the amplifier in the fine conversion and loop filtering phases, respectively. D_{NS} represents the fine conversion result, and E_2 is the quantization error. With the feedforward path, D_{NS} can be calculated as

$$\begin{aligned} D_{\mathrm{NS}} &= -E_1 + V_{\mathrm{IN}}(t_2) - V_{\mathrm{IN}}(t_1) \\ &\quad + \frac{E_2}{1 + H_{\mathrm{IIR}}} - v_{\mathrm{ns1}} + \frac{v_{\mathrm{ns2}}}{G} \\ &\quad + v_{\mathrm{namp,ktc}} + \frac{v_{\mathrm{namp,lf}} \cdot H_{\mathrm{IIR}}}{1 + H_{\mathrm{IIR}}} + \frac{v_{\mathrm{amp,conv}}}{1 + H_{\mathrm{IIR}}}. \end{aligned} \tag{3}$$

Therefore, the ADC conversion result D_{OUT} can be obtained by directly combining D_{DS} and D_{NS}

$$\begin{aligned} D_{\mathrm{OUT}} &= D_{\mathrm{DS}} + D_{\mathrm{NS}} \\ &= V_{\mathrm{IN}}(t_2) + \frac{E_2}{1 + H_{\mathrm{IIR}}} + \frac{v_{\mathrm{ns2}}}{G} \\ &\quad + v_{\mathrm{namp,ktc}} + \frac{v_{\mathrm{namp,lf}} \cdot H_{\mathrm{IIR}}}{1 + H_{\mathrm{IIR}}} + \frac{v_{\mathrm{amp,conv}}}{1 + H_{\mathrm{IIR}}}. \end{aligned} \tag{4}$$

As can be seen, the amplifier noise requirement differs in the three phases. The amplifier noise in fine conversion can be shaped by the loop filter, and thus, the amplifier's noise requirement can be relaxed. In contrast, the amplifier noises in both kT/C noise cancellation and loop filtering are critical. With the skipped sampling scheme, one-shot incremental zoom conversion requires eight times sampling and 32 times loop integration, leading to different amplifier noise averaging effects in these two phases. As a result, the amplifier noise in kT/C noise cancellation demonstrates higher significance compared to that in loop filtering. To accommodate these different noise requirements while offering high system-level energy efficiency, the three-mode reconfigurable FIA is designed.

C. Three-Mode Reconfigurable FIA

The system power consumption is dominated by the amplifier, which enables kT/C noise cancellation, fine conversion, and loop filtering during the ADC operation. Based on the noise analysis in Section II-B, the amplifier's noise performance can be designed accordingly in the three phases for power reduction.

In this work, the FIA structure is adopted as the embedded amplifier due to its simplicity, energy efficiency, and stable common mode. The FIA's input-referred noise can be expressed as [23]

$$v_{\mathrm{namp}}^2(t_{\mathrm{amp}}) = \frac{2nkT}{C_{\mathrm{RES}} \cdot \Delta V_S(t_{\mathrm{amp}})} \cdot \frac{I_D}{G_m} \tag{5}$$

where t_{amp} is the amplification time, C_{RES} is the reservoir capacitance, $\Delta V_S(t_{\mathrm{amp}})$ is the input pair's source voltage change, and G_m represents the input pair's total transconductance.

As can be seen, the input-referred noise of FIA is inversely proportional to C_{RES} and G_m/I_D. Therefore, to realize different noise performance in the three phases, a three-mode reconfigurable FIA is designed, as shown in Fig. 5. During the sampling phase, the most noise-critical phase, a large reservoir capacitor of 16 pF is adopted for kT/C noise amplification. An amplification time of 16 ns is allocated to improve G_m/I_D with deep quenching, leading to an input-referred FIA noise of 19.8 μVrms. With relaxed noise requirements in the loop filtering and fine conversion phases, smaller reservoir capacitors can be adopted for energy saving. In this design, the FIA's reservoir capacitor is reduced to 9 pF for loop filtering and to only 1.5 pF for fine conversion. Meanwhile, the amplification time is reduced accordingly, yielding input-referred noise of 30.9 and 44.1 μVrms in these two phases. As a result, the amplifications for the loop filtering and fine conversion consume only 50% and 15% energy, respectively, compared to that for kT/C noise cancellation.

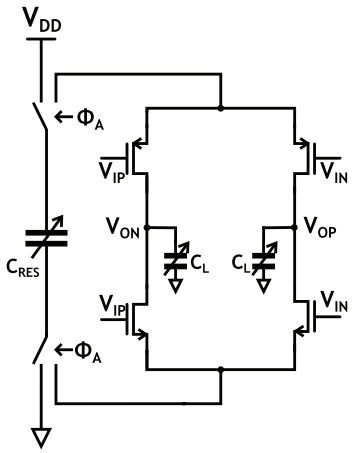

Fig. 5. Schematic of the proposed three-mode reconfigurable FIA.

TABLE I
SUMMARY OF THE THREE-MODE RECONFIGURABLE FIA

FIA Mode	Reservoir Cap. [pF]	Load Cap. [pF]	Gain	Input-referred Noise [Vrms]
kT/C Noise Amplification	16	5 (C_{LS}+C_{LL}+C_{NC})	10.7	19.8μ
Loop Filtering	9	2.5 (C_{LS}+C_{LL})	10.8	30.9μ
Fine Conversion	1.5	0.5 (C_{LS})	10.7	44.1μ

To maintain a constant gain for the amplifier across these three phases, the load capacitance of the FIA varies accordingly in these three phases. In addition to the always-connected small capacitor C_{LS}, an extra load capacitor C_{LL} is added during kT/C noise amplification and loop filtering, and the noise cancellation capacitor C_{NC} also serves as the FIA's load capacitor during the kT/C noise amplification. As shown in Table I, by appropriately designing the capacitance values of C_{LS}, C_{LL}, and C_{NC}, a relatively constant FIA gain of 10 is realized in this work based on the simulation results.

Similar to the noise performance, the amplifier's gain among the three phases shows a similar accuracy requirement. As the simulation results shown in Fig. 6, compared to the FIA's gain

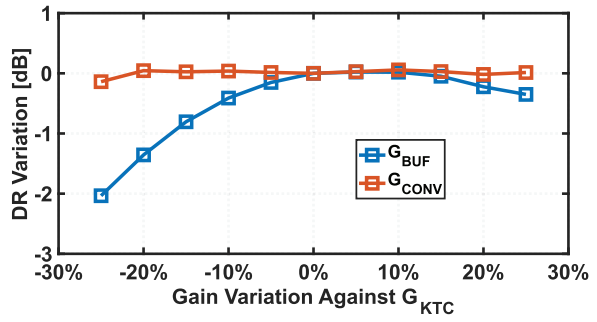

Fig. 6. Simulated system performance variation versus FIA gain variation against G_{KTC}.

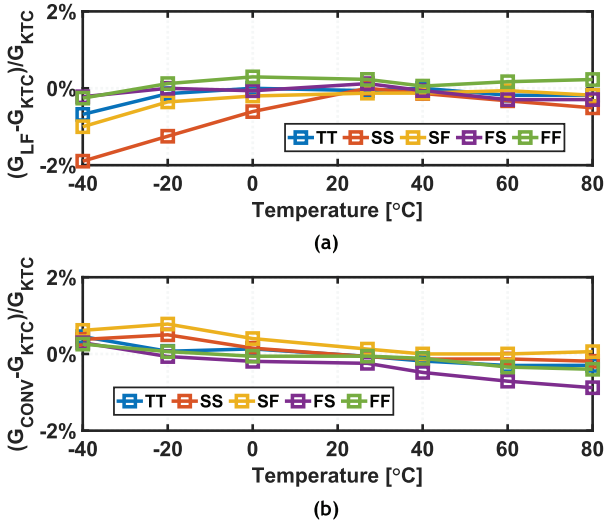

Fig. 7. Simulated FIA gain variations under process corner and temperature variations in (a) loop filtering phase and (b) fine conversion phase.

during kT/C noise amplification (G_{KTC}), ±10% gain variation in the loop filtering phase (G_{LF}) leads to a maximum of 0.5-dB performance degradation. The fine conversion phase (G_{CONV}) can tolerate over ±25% gain variation. In this work, a one-time trimming is performed using a 3-b trimming bank with a total capacitance of 2 pF, and the trimming bank is connected in parallel with the reservoir capacitor for gain centering during loop filtering [24]. After gain centering at 27 °C, with the temperature varying from −40 °C to 80 °C in different corners, the variation of both G_{LF} and G_{CONV} can be within ±2%, as shown in Fig. 7. Consequently, the three-mode reconfigurable FIA can satisfy performance requirements across all modes while maintaining excellent energy efficiency.

III. Proposed Single Buffer Embedded NS-SAR Fine Quantizer

As the resolution-critical block in the zoom architecture, the NS-SAR quantizer demands a robust and sharp noise transfer function (NTF) while maintaining low hardware and power costs. The key to realize that is to design an efficient, high-performance, and robust loop filter. This section will first briefly review some prior loop filter designs, followed by the introduction of the proposed single buffer embedded loop filter design adopted in this work.

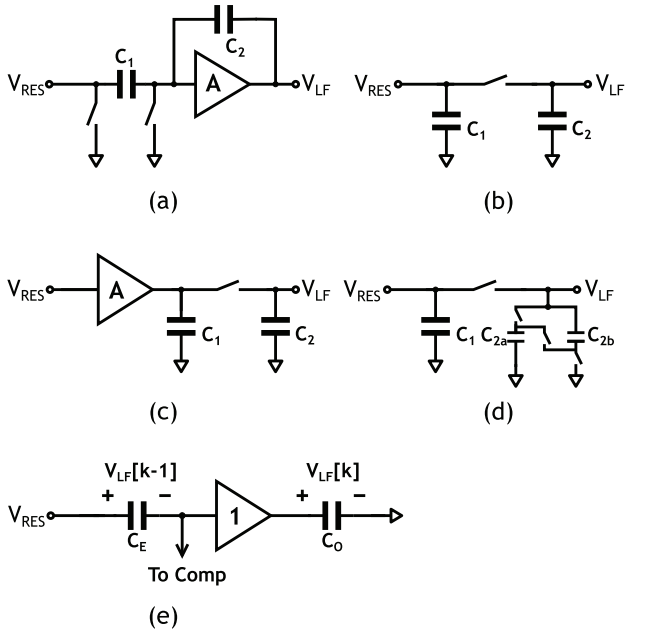

Fig. 8. Simplified schematic of prior loop filter designs. (a) OTA-based loop filter in [25]. (b) Charge sharing-based fully passive loop filter in [26]. (c) Charge sharing-based loop filter with open-loop amplifier in [27]. (d) Charge sharing-based loop filter with passive gain in [28]. (e) Capacitor stacking-based loop filter in [18].

A. Review of Prior Loop Filter Designs

Various loop filter designs have been explored for NS-SAR ADCs, as shown in Fig. 8. The early designs employed the closed-loop amplifier-based integrator like conventional ΔΣMs [25]. It offers robust and sharp NTF while consuming considerable power due to high-gain amplifiers. The fully passive loop filter is adopted in [26] featuring high energy efficiency and low hardware cost. However, limited by the signal attenuation during the charge sharing, it is difficult to realize a sharp NTF. Several methods have been proposed to resolve the signal attenuation by introducing dedicated gain stages, such as pre-amplifying the residue before the fully passive loop filter using an open-loop amplifier [27] or providing additional passive gain after it [28]. Yet, the open-loop amplifier is process, voltage, temperature (PVT)-sensitive, while the passive gain stage suffers from limited gain value. In [18], a capacitor stacking-based integrator is proposed. By using dynamic buffers for residue extraction, no charge sharing is introduced, thereby realizing a robust and sharp NTF. Nevertheless, N dynamic buffers are needed for an Nth-order loop filter, causing extra hardware cost and power consumption.

B. Proposed Single Buffer Embedded Loop Filter

In this work, a single buffer embedded loop filter is proposed to meet the design requirement, in which only one dynamic buffer is required to realize the second-order loop filter. As shown in Fig. 9, in the $(k-1)$th conversion cycle, the dynamic buffer extracts the integration voltage $V_{INT}[k-1]$, which is stored on two capacitors in parallel. No charge sharing and signal attenuation occur during the extraction. In the kth

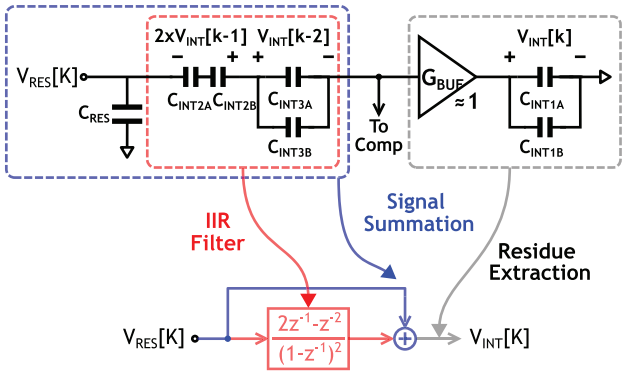

Fig. 9. Schematic and signal diagram of the proposed single buffer embedded loop filter.

conversion cycle, these two capacitors are stacked in series to realize a passive gain of 2. Together with the reversely connected capacitors from $(k-2)$th cycle, the extracted integration value of kth conversion cycle $V_{\mathrm{INT}}[k]$ can be calculated as

$$V_{\mathrm{INT}}[k] = G_{\mathrm{BUF}} \cdot (V_{\mathrm{RES}}[k] + 2 \cdot V_{\mathrm{INT}}[k-1] - V_{\mathrm{INT}}[k-2]) \tag{6}$$

where G_{BUF} is the buffer gain. By rotating these capacitors, the second-order integration can be achieved. The loop filter's transfer function H_{LF} can be calculated as

$$H_{\mathrm{LF}} = \frac{V_{\mathrm{INT}}}{V_{\mathrm{RES}}} = \frac{G_{\mathrm{BUF}}}{1 - G_{\mathrm{BUF}} \cdot (2z^{-1} - z^{-2})}. \tag{7}$$

Assuming an ideal buffer gain of 1, the signal diagram can be depicted accordingly in Fig. 9, which demonstrates its second-order integration capability together with an inherent feedforward path.

During the loop filtering, the signal gain and summation are realized by capacitor stacking, which is accurate and PVT robust. The only active component that affects NTF is the dynamic buffer. A duty-cycled flipped voltage follower (FVF)-based buffer is adopted as the dynamic buffer due to its simplicity, high driving capability, and good energy efficiency. Its noise can be attenuated by the FIA, and thus, a low-power FVF design is adopted. As shown in Fig. 10(a), a buffer gain of over 0.93 can be guaranteed over a large temperature range and process corners. The sufficient gain results in sharp NTFs, as shown in Fig. 11. Simulation results in Fig. 10(b) demonstrate a signal-to-quantization-noise ratio (SQNR) beyond 103 dB. Therefore, a robust and effective NS effect can be realized using the proposed single buffer embedded loop filter. Note that with this architecture, one can easily increase the NS order without requiring extra buffers.

IV. Circuit Implementation

The simplified top-level schematic and the timing diagram of the proposed incremental zoom ADC are shown in Fig. 12. It comprises a 6-b DS coarse quantizer and a 7-b NS-SAR fine quantizer. The split-capacitor array is adopted in both coarse and fine DACs to ensure a stable common-mode voltage during the whole conversion [29]. The unit capacitance in

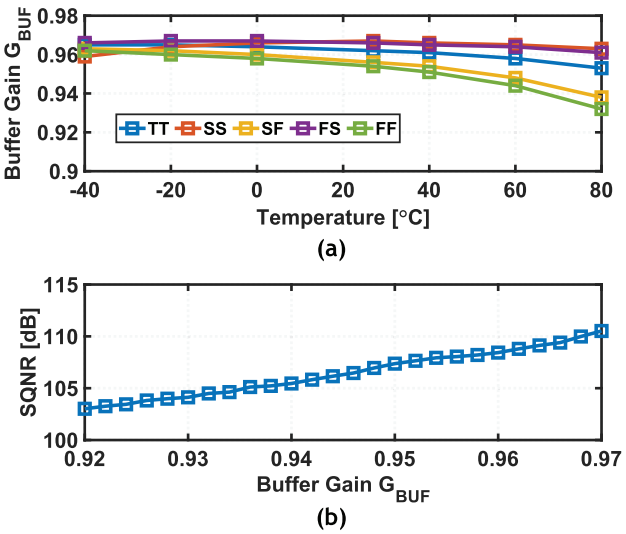

Fig. 10. (a) Simulated FVF-based buffer's gain with process corner and temperature variations. (b) Simulated system performance variation versus buffer's gain.

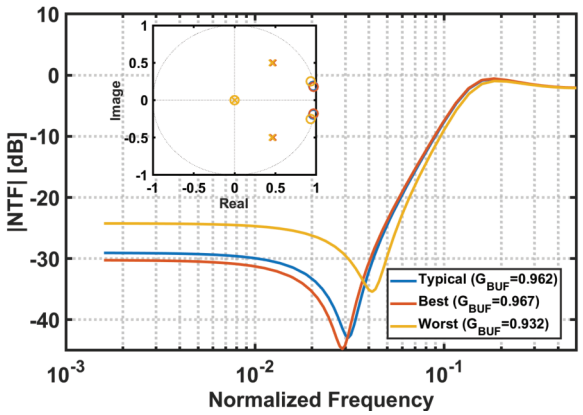

Fig. 11. Magnitude and pole/zero locations of the NTF.

the merged DAC is 1 fF. The coarse DAC is thermometer-coded, where C_1 is 12 fF, comprising 12 unit capacitors. An additional $0.5C_1$ is added to the coarse DAC to help center the coarse residue voltage around zero after slope operation. The fine DAC is binary-coded, with the last 2 bits realized using bridge capacitors; it results in an equivalent minimum capacitance C_2 of 0.25 fF. During the sampling phase, the input signal is bottom-plate sampled on the capacitive digital-to-analog converter (CDAC). The kT/C noise cancellation is performed using the FIA; thus, the CDAC can be reduced to 0.8 pF, largely relaxing the input and reference driving requirements. Compared to the prior kT/C noise cancellation scheme [21] where a static amplifier is used, the FIA operates in a fully dynamic fashion, leading to significant energy saving.

During the coarse conversion phase, the DS quantization is performed [30], which features lower DAC switching energy compared to the binary search as in the conventional SAR quantizer. However, in conventional DS quantizer design, 2^N conversion cycles are required for N-bit resolution, limiting the quantization speed, as shown in the gray line of Fig. 13(a).

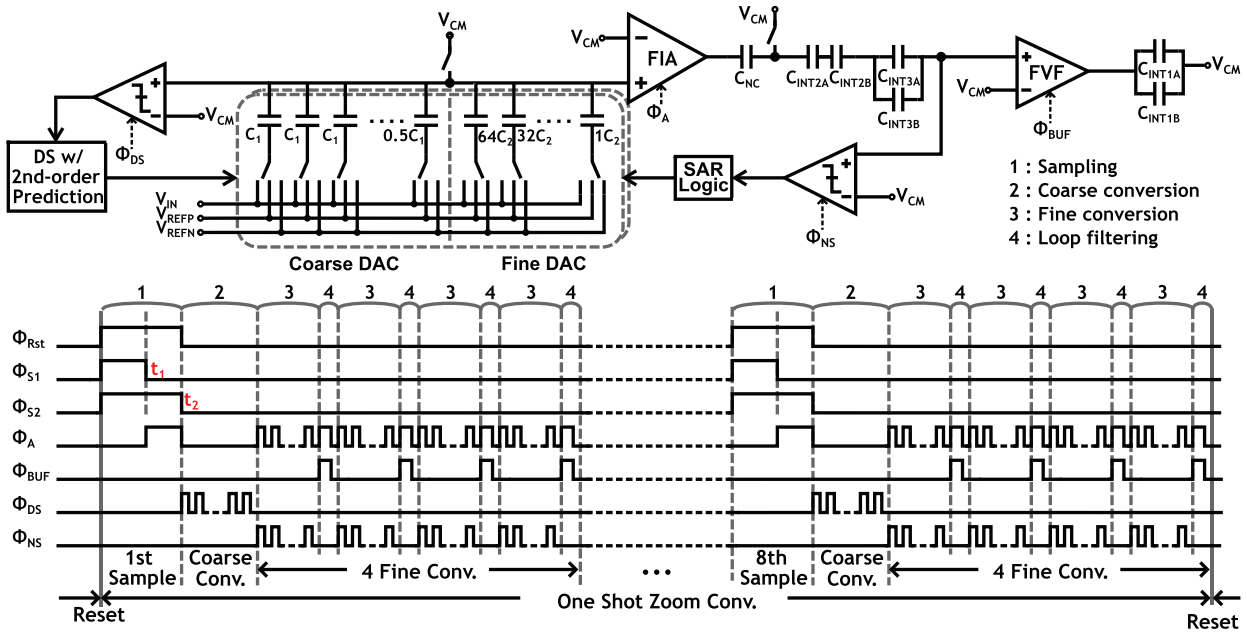

Fig. 12. Simplified schematic and timing diagram of the proposed incremental zoom ADC.

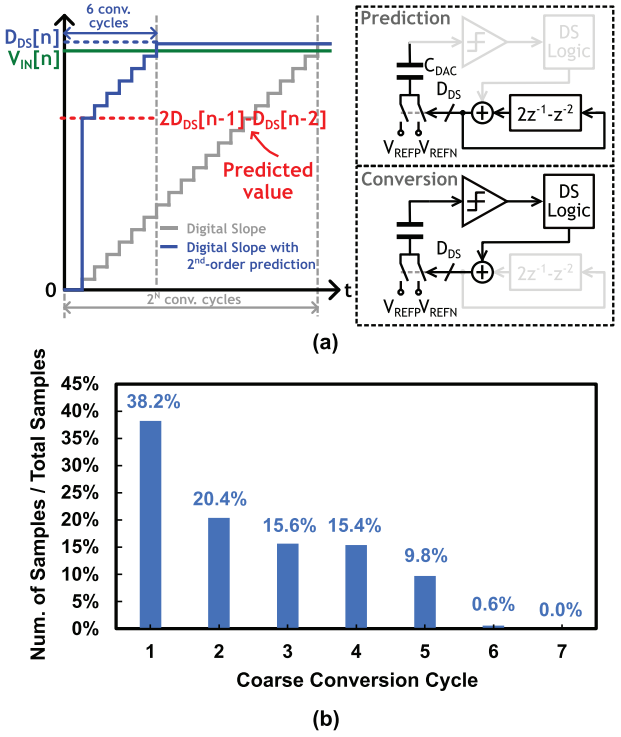

Fig. 13. (a) Schematic and operations of the DS coarse quantizer with the second-order digital prediction. (b) Simulated coarse conversion cycles for full-scale Nyquist input.

Given that the input has a limited bandwidth in the oversampled system, it leads to small input signal changes between the consecutive samplings. As a result, the ADC's consecutive coarse conversion results differ by only several LSBs, making it possible to incorporate a digital prediction process before the coarse conversion starts [31]. After the nth input sampling, the predicted coarse conversion result $2 \cdot D_{\mathrm{DS}}[n-1] - D_{\mathrm{DS}}[n-2]$ is applied directly to the coarse DAC's bottom-plate switches. Then, during the coarse conversion, the 6-b DS coarse quantizer equivalently converts the differences between the sampled input signal and the predicted value. In each bit conversion cycle, the DS logic switches only one unit capacitor up or down by adding or subtracting 1 to the predicted value, with a low reference driving cost. As shown in the blue line of Fig. 13(a), the DS conversion continues until the D_{DS} reaches the sampled input signal $V_{\mathrm{IN}}[n]$, yielding a coarse conversion result of $D_{\mathrm{DS}}[n]$ in six conversion cycles. The difference between $V_{\mathrm{IN}}[n]$ and the predicted value $2{\cdot}D_{\mathrm{DS}}[n{-}1]{-}D_{\mathrm{DS}}[n{-}2]$ varies from sample to sample, causing D_{DS} to require a different number of conversion cycles to reach $V_{\mathrm{IN}}[n]$. The required conversion cycles also depend on the input amplitude and frequency. With a full-scale Nyquist-frequency input signal, the required conversion cycles are counted among 40000 samples, as shown in Fig. 13(b). It indicates that a maximum of six conversion cycles are required for the DS operation, demonstrating the fast input tracking capability for Nyquist input. As a result, the proposed digital-slope quantizer with the second-order digital prediction offers both fast input tracking and low DAC switching energy.

During the fine conversion phase, the 7-b NS-SAR fine quantizer converts the amplified coarse residue voltage. The total capacitance of the fine DAC is five times larger than C_1 in the coarse DAC, providing four LSBs' inter-stage redundancy. Calculated using a Nyquist-frequency input, the signal difference stored on C_{NC} during the kT/C noise cancellation is within one LSB. After fine conversion, the FVF extracts the integration value and updates the loop filter. Each capacitor (C_{INT}) in the loop filter is designed as 500 fF to mitigate the impact of parasitic capacitance from the switches. After that, thanks to the charge conservation on CDAC, the fine DAC's bottom plate can be reset to regenerate the coarse residue voltage without resampling. As a result, multiple fine conversions can be performed after a single input sampling

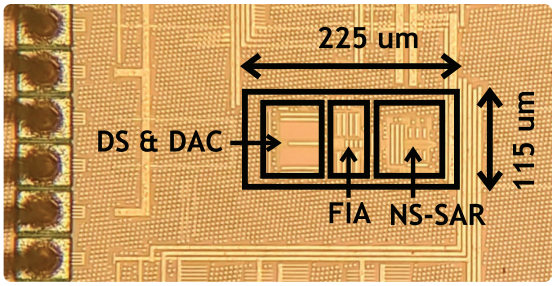

Fig. 14. Chip micrograph of the proposed incremental zoom ADC.

and coarse conversion. However, the loop filter's parasitic capacitor shares a small amount of charge with the C_{NC} during each fine conversion. Increasing the number of fine conversions per sampling would exacerbate charge depletion on the C_{NC}. Therefore, four consecutive fine conversions are performed in this work to minimize charge sharing and reduce the sampling operations by four times. With a small OSR of 8 to average the FIA's thermal noise during kT/C noise amplification, a total of 32 conversion cycles can be performed to achieve high quantization accuracy.

Overall, the proposed ADC offers easy drive capability for both the input and reference signals: 1) input and reference driving requirements are both relaxed due to the small capacitance of CDAC thanks to kT/C noise cancellation; 2) with the proposed skipped sampling scheme, fewer sampling operations are needed for one-shot incremental zoom conversion, thus reducing the input current and driving cost; and 3) using the proposed digital-slope coarse quantizer with the second-order prediction, the DAC switching activities are minimized, thereby reducing the reference power consumption.

In addition, by adopting the proposed three-mode reconfigurable FIA and single buffer embedded NS-SAR quantizer, the ADC core achieves high resolution while maintaining good energy efficiency.

V. Measurement Results

The prototype ADC is fabricated in a 28-nm CMOS. Fig. 14 shows the chip micrograph. The ADC core occupies an active area of 0.026 mm^2. Fig. 15 shows the measured output spectra. The capacitor mismatch is foreground calibrated once before all measurements. At a low input frequency of 2.5 kHz, the measured SFDR and SNDR are 107.2 and 92.5 dB, respectively. The SFDR of the proposed ADC is mainly limited by the second-order distortion due to P/N mismatch and third-order distortion. The tone at ~100 kHz is aroused from the test setup. At a high input frequency of 147 kHz, the measured SFDR is 101.5 dB, proving the ADC's easy-input-driving feature and the Nyquist tracking capability of coarse DS quantizer with second-order digital prediction. The measured SNDR is 89.5 dB, which is 3 dB lower than that measured at low frequency. The SNDR degradation is primarily attributed to the signal attenuation caused by the decimation filter, which is also present in other NS ADCs that account for the digital output filter. Fig. 16 shows the signal transfer function (STF) of the employed second-order decimation filter, normalized

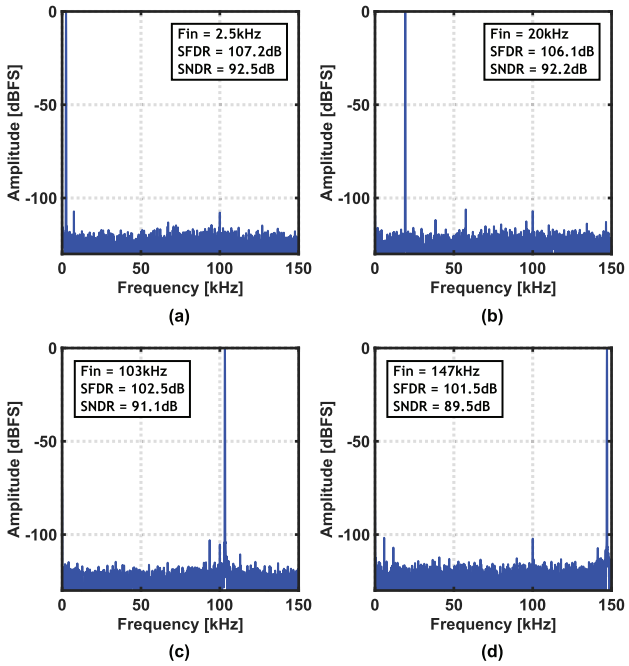

Fig. 15. Measured output spectra with (a) 2.5-, (b) 20-, (c) 103-, and (d) 147-kHz inputs.

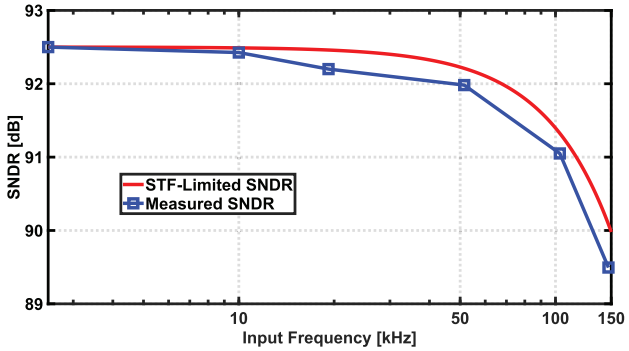

Fig. 16. Measured SNDR versus input frequency.

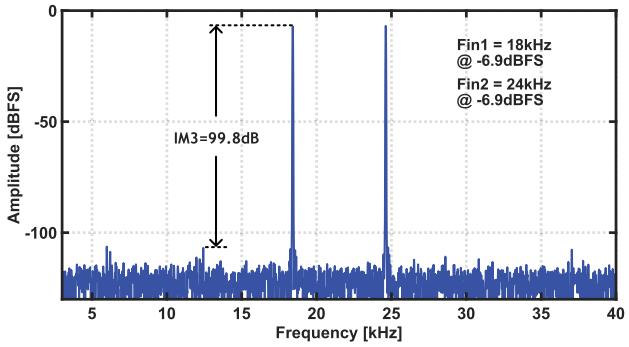

Fig. 17. Measured output spectra with two-tone input.

to the low-frequency SNDR of 92.5 dB, indicating a signal attenuation of 2.5 dB at 150 kHz. The audio-frequency two-tone test in Fig. 17 shows an IM3 of −99.8 dB. As illustrated in Fig. 18, the SNDR is measured under ±10% analog supply voltage variation and a temperature range of −20 °C–80 °C to validate robustness, demonstrating a <2-dB SNDR variation. The SNR/SNDR versus input amplitude in Fig. 19 shows a

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ADCS

	ISSCC-18 P. Vogelmann	ISSCC-21 Liu	ISSCC-24 Cheng	ISSCC-16 Gonen	VLSI-20 Eland	ISSCC-22 Liu	**This work**		
Architecture	Incremental ΔΣ	NS-SAR	NS-SAR	Dynamic Zoom	Dynamic Zoom	Incremental Zoom (SAR+ΔΣ)	**Incremental Zoom (DS+NS-SAR)**		
Process [nm]	180	40	28	160	160	55	**28**		
BW [kHz]	100	250	100	20	20	Quasi-static	**150**		
Conv. Cycles	--	--	--	--	--	128	**32**		
OSR	150	10	25	282.25	87.5	128	**8**		
Sample cap [pF][2]	16	16	12	4.96	6.8	4	**0.8**		
Equiv. sample cap [pF]	2400	160	300	1400	595	512	**6.4**		
Reference [V]	3	1.1	1	1.8	1.8	1	**1**		
Area [mm^2]	0.363	0.094	0.09	0.16	0.27	0.23	**0.026**		
Power [uW]	1098	340	107.38	1650	440	4.96	**160**		
Input Frequency [kHz]	13	49	9	1	1	0	**2.5**	**20**	**150**
SNDR [dB]	86.6	93.3	94.3	98.3	106.5	93	**92.5**	**92.2**	**89.5**
FoMw^2 [fJ/c-s]	314.2	18.0	12.6	613.7	63.7	50.2	**15.6**	**16.0**	**21.8**
FoMs^3 [dB]	166.2	182	184	169.1	183.1	177.3	**182.2**	**181.9**	**179.2**

[1]Equivalent sample capacitance = sample cap x OSR, representing the total sampled capacitance for one conversion.
[2]FoMw=Power/(2^{ENOB}·2·BW)
[3]FoMs=SNDR+10·$\log_{10}$(BW/Power)

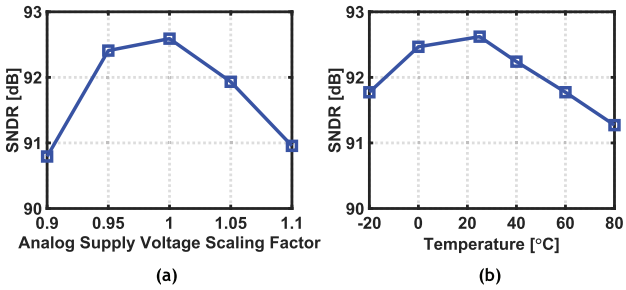

Fig. 18. Measured SNDR versus (a) analog supply voltage and (b) temperature variations.

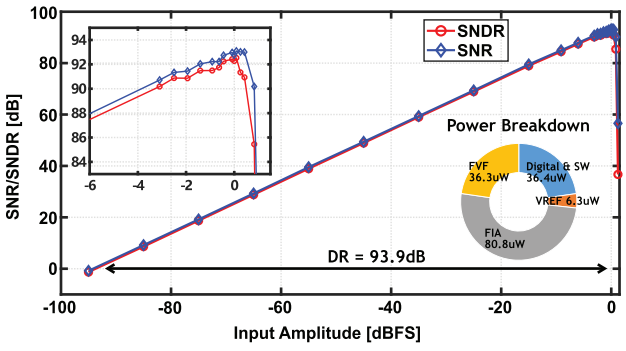

Fig. 19. Measured dynamic range and power breakdown.

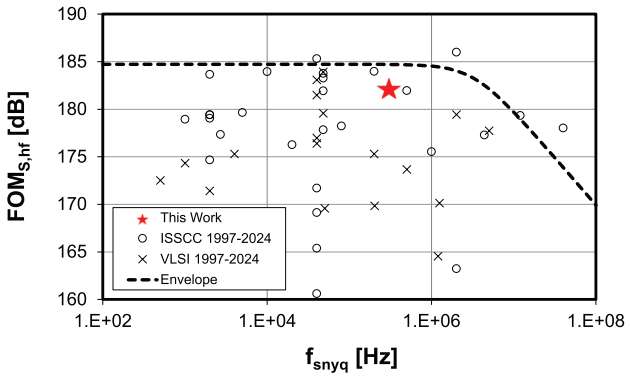

Fig. 20. High-resolution ADC survey [32].

DR of 93.9 dB. The ADC core consumes 160 μW at 300 kS/s from a 1-V supply, including 80.8 μW for the three-mode reconfigurable FIA, 36.3 μW for the FVF-based dynamic buffer, 36.4 μW for digital and switches, and only 6.3 μW for the reference due to the small CDAC capacitance and minimum DAC switching activities. The ADC noise and power performance are both dominated by the FIA.

Table II summarizes the performance of this work and compares it with prior publications. Thanks to the kT/C noise cancellation and the proposed skipped sampling scheme, among discrete-time ADCs with similar performance (>90 dB SNDR), this work has the minimum equivalent sampling capacitance, which represents the total sampled capacitance for one conversion. By adopting the efficient NS-SAR as the fine quantizer, this design only requires a low conversion cycle of 32 and an OSR of 8. Therefore, it achieves a medium conversion speed of 300 kS/s. Combining

all these merits, this work also achieves a superior FoMw of 15.6 fJ/c-s and FoMs of 182.2 dB, as illustrated in the high-resolution (>90 dB SNDR) ADC survey in Fig. 20.

VI. Conclusion

This article proposes an incremental zoom ADC for loT applications, which features easy driving characteristics with high precision, medium bandwidth, and state-of-the-art energy efficiency. By employing the proposed skipped sampling scheme, multiple fine conversions can be performed consecutively without repeated sampling operations, reducing the driving costs and conversion period. A DS ADC with a second-order prediction is adopted as the coarse quantizer for low DAC switching energy and fast input tracking. A second-order NS-SAR quantizer is proposed as the fine quantizer to reduce the required conversion cycles and increase the conversion speed. It only requires one dynamic buffer, ensuring high energy efficiency. Moreover, with this architecture, the NS order can be easily increased without requiring extra buffers. An amplifier-reused kT/C noise cancellation technique is also enabled to ensure sampling precision under a low OSR of 8. Combining all the merits, this work realizes a 92.5-dB SNDR at 300 kS/s while consuming only 160 μW, leading to a superior FoM of 182.2 dB.

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